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COATS & BENNETT, PLLC
P O BOX 5
RALEIGH, NC 27602

EXAMINER	
WANG, TED M	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 05/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/747,052	HAM, EUGENE D.	
	Examiner	Art Unit	
	Ted M. Wang	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-16,18,24-26,32-35,37 and 39* is/are rejected.

7)☒ Claim(s) *8,9,17,19-23,27-31,36 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed on 03/01/2006, have been fully considered but they are not persuasive. The Examiner has thoroughly reviewed Applicants' arguments but firmly believes that the cited reference to reasonably and properly meet the claimed limitations.

Independent Claims 1, 10, and 24

(1) *Applicants' argument –*

(a) "Applicant's claim limitations involving PLL output signal generation. Tanaka's illustrations and its description of NCO 9 at col. 5, lines 43-52 irrefutably contradicts the Office's assertion that the signal generated by NCO 9 can "inherently' be taken as an "output signal" within the meaning of Applicant's claims. The signal generated by NCO 9 may be an output signal with respect to NCO 9, but it is not an output signal of the AFC / PLL circuit in which NCO 9 resides, nor would one skilled in the art ever understand the NCO 9 signal as an output signal. Indeed, Tanaka plainly illustrates the DEMODULATED SIGNAL output by phase detector 10 as its AFC / PLL output signal, and the Office does not account for this contradiction to its arguments." as recited;

(b) "First, as argued extensively above, element 9 does not produce the claimed PLL output signal, therefore element 8, which is disclosed only as receiving signals from elements 6 and 9 cannot by definition produce the claimed successive phase differences between PLL input and output signals. Second, as explicitly explained by

Tanaka at col. 5, line 13-26, the output of the (loop) filter 11 is proportional to the oscillation frequency of NCO 9, rather than being a function of successive control values within the meaning of Applicant's claims. Further, Tanaka discloses that filter 11 is updated not as a function of average control values, but rather as a function of a time change amount $\Delta g(nT)$, which is determined by a delaying device 13, a subtracting circuit 14, and an averaging circuit 15. While the Office argues that this is the same as Applicant's claimed averaging-based control, that argument glosses over differences which cannot be overlooked in an anticipation analysis. That is, Tanaka explicitly teaches the output of filter 11 as being proportional to the oscillator frequency of NCO 9, not proportional to successive phase differences between input and output signals. Further Tanaka explains that filter 11 is updated by subtracting a delayed version of the filter 11 output signal from a current version. It is these "delta" signal values which are averaged by averaging circuit 15 to produce the filter adaptation of Tanaka." as recited; and

(c) "Applicant respectfully requests that the Patent Office provide technically detailed arguments that are consistent with the teachings of Tanaka." as recited,

Examiner's response –

In response to applicant's argument as described above, the applicant argued that the signal generated by NCO 9 can not "inherently" be taken as an "output signal" within the meaning of applicant's claims and request examiner provide technically detailed arguments that are consistent with the teaching of Tanaka. The examiner's response follows.

It is well know in the field of communication system that a PLL has the following structure (Fig.A).

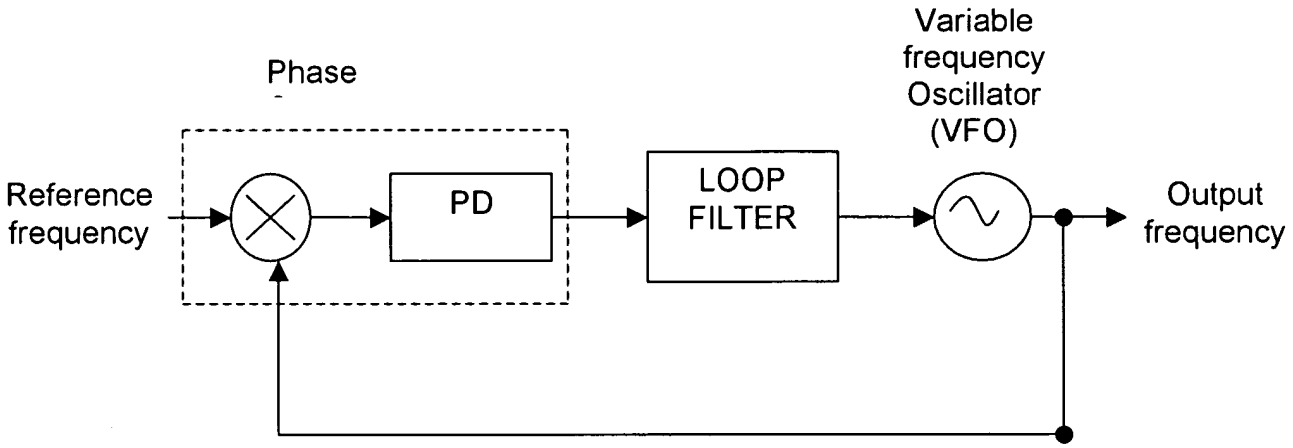

Figure A

The PLL circuit is arranged to have a phase comparator being inputted with a reference frequency, a low-pass filter (or Loop filter), and a variable frequency oscillator (VFO). The output from the VFO is taken as a PLL output signal (frequency) at an output terminal as well as sent back to the phase comparator 102. ***The VFO normally uses a voltage controlled oscillator (VCO) for the analog PLL, while for the digital PLL, the VFO uses an oscillator arranged to change a frequency dividing ratio according to input phase error information, such as a number controlled oscillator (NCO)***.

In operating, the phase comparator operates to compare the PLL output signal with the input signal. Then, the compared result (successive phase difference values) is sent to a Loop Filter through which a dc signal corresponding to the phase difference is taken out. Based on the phase difference signal, the oscillating frequency of the

VFO is controlled so that the resulting PLL output signal takes synchronization with the input reference signal.

As shown in Fig.3, Tanaka teaches an analog PLL circuit (elements 17-20) with a voltage controlled oscillator (VCO) 20. Tanaka further teaches a digital PLL circuit (elements 8-11, 13-16, 101 and 102) with a numeric controlling oscillator (NCO) 26 in Fig.1. Fig.3 and Fig.1 of Tanaka's reference can be redrawn in the form of Fig.A basic PLL circuit block diagram as Figure B and Figure C, respectively. As we can easily seeing that *both **Fig.3 and Fig.1** of the PLL circuits have the exact same structure as that of **Figure A as shown** above. That is, the **Fig.3 (Fig.B)** of PLL circuit is an analog PLL with a VCO and **Fig.1 (Fig.C)** of PLL circuit is a digital PLL with a NCO.*

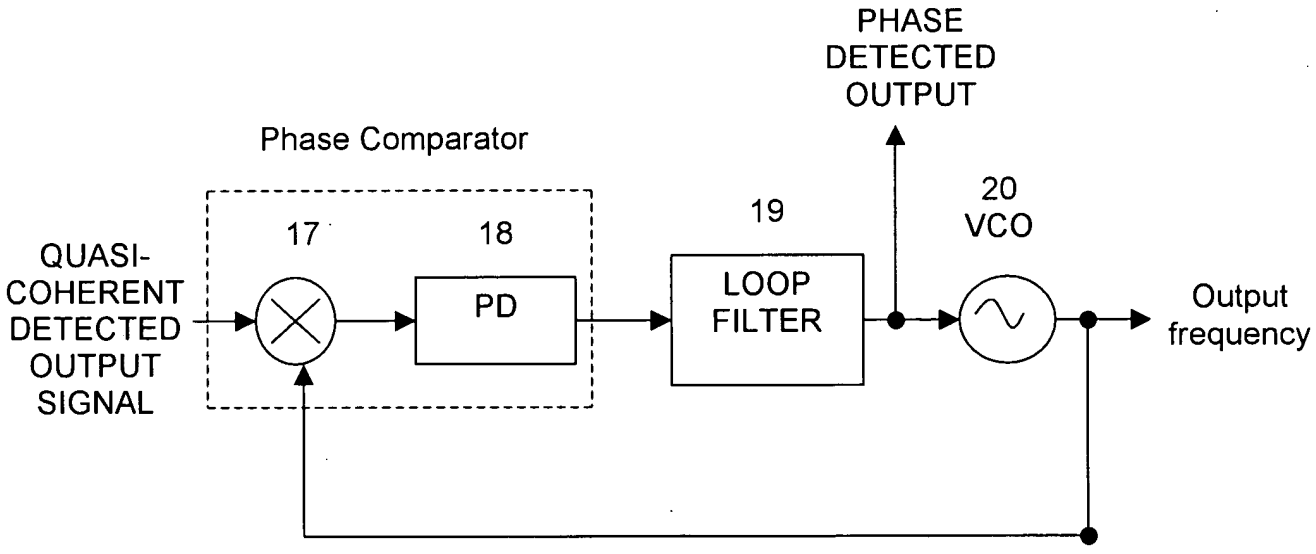

Figure B

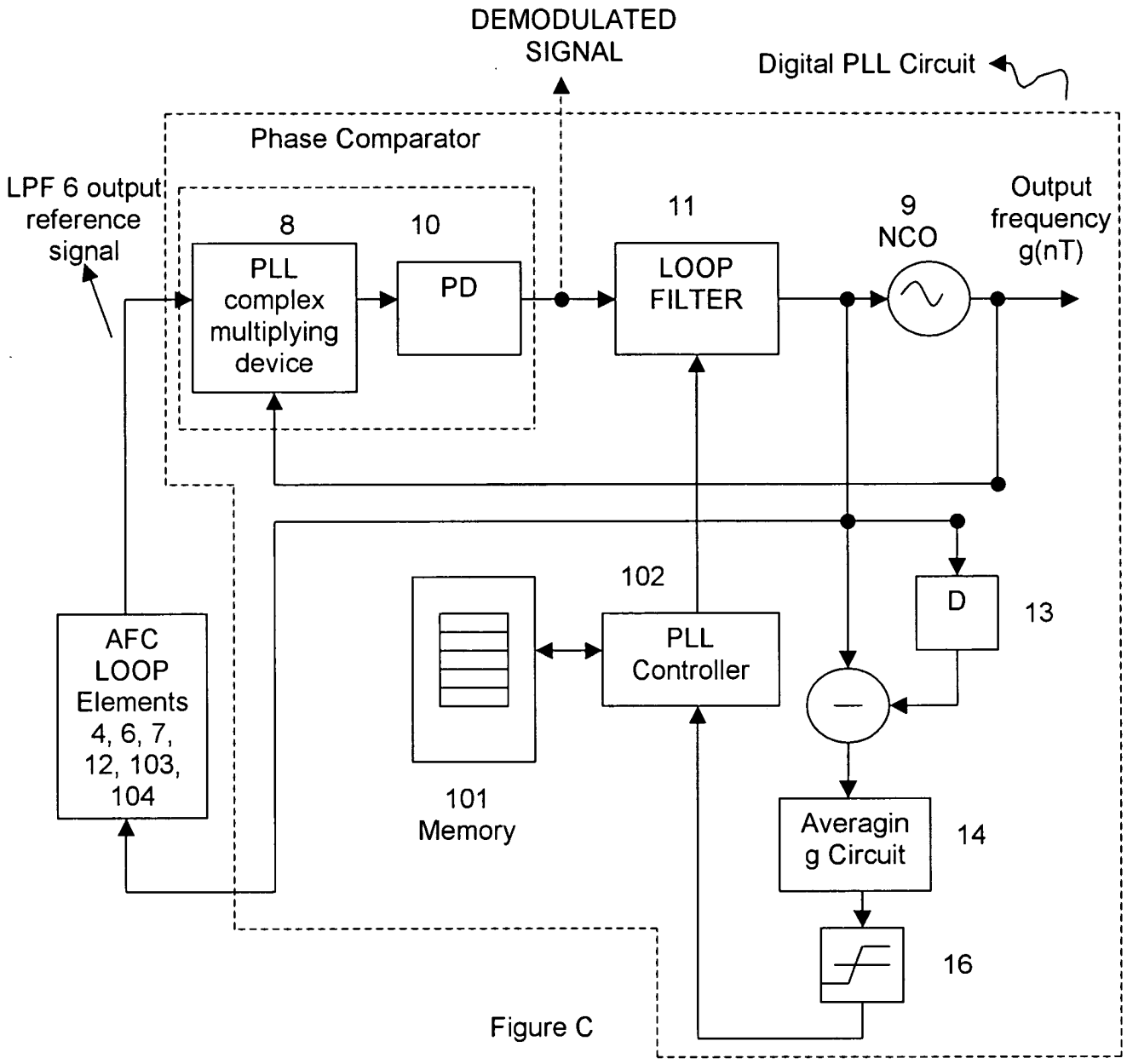

Figure C

The operation of Fig.3 (or Fig.B) analog PLL is described in column 1 line 25 – column 2 line 6 and the operation of Fig.1 (or Fig.C) digital PLL is described in column 3 line 58 – column 4 line 18, column 4 line 43 – column 5 line 14, and column 5 line 40 – column 6 line 24 of the Tanaka's reference.

Refer back to Fig.C, the NCO 9 output signal in not only with respect to NCO 9, but also with respect to the digital PLL.

Applicant also argued that the output of the (loop) filter 11 is proportional to the oscillation frequency of NCO 9, rather than being a function of successive control values within the meaning of Applicant's claims. In response this argument, examiner refers to Fig.1 (Figure C) of the Tanaka's reference again. The adjustable loop filter 11 output g(nT) provides successive control values to the delayed element 13 and subtractor 14 and outputs a signal having a function of $\Delta g(nT)$, then the averaging circuit 15 averages the function of $\Delta g(nT)$ signal. The data determining device 16 compares the averaged signal with a threshold and outputs the determined signal to the PLL controller 102 to select the parameters of the loop range, the frequency control width, and the control time interval of the PLL corresponding to the output signal of the data determining unit 16 so as to control the PLL filter 11 (column 5 line 42 – column 6 line 6).

As admitted in the applicant's argument, the loop filter 11 is updated as a function of $\Delta g(nT)$ which is determined by a delaying device 13, a subtracting device 14, and an averaging circuit 15. Examiner cites column 5 equation 8 to show that the time change amount $\Delta g(nT)$ is a function of the successive phase difference values g(nT) and a function of the delayed successive phase difference values g(nT-T). i.e. $\Delta g(nT) = g(nT) - g(nT-T)$.

With this simple equation, it is inherent for one of ordinary skill in the art at the time of the invention was made should recognize $\Delta g(nT)$ is a function of the successive

phase difference values g(nT) and the loop filter 11 is updated also as a function of average control value (output of averaging device 15) determined from the successive control value g(nT).

Thus, for the explanation addressed in the above paragraph, the rejection under 35 U.S.C. 102(b) with Tanaka's reference is adequate.

In further, if the applicant does not agree that the NCO 9 output signal is not related to PLL generate output that is a basic PLL circuit structure, applicant should provide the technically detailed arguments to differentiate the instant application's PLL circuit theory to the basic PLL circuit theory provided in this argument.

Claim Objections

2. Claim 24 is objected to because of the following informalities:

- Claim 24, line 1, after "loop" insert --- PLL ---.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-7, 10, 11, 13-16, 18, 24-26, 32, and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka (US 5,909,148).

- With regard claim 1, Tanaka discloses a method of generating an output signal from a phase-locked loop (PLL), comprising

  determining successive phase difference values (Fig.1 elements 8 and 10) between a reference clock signal (Fig.2 element 6 output) and said output clock signal (Fig.1 element 9 output, where it is inherent that the NCO output can be taken as an output clock signal.);

  filtering said successive phase difference values to generate successive control values (Fig.1 element 11);

  controlling a frequency of said output clock signal based on said successive control values (Fig.1 element 13, 14, 15, 16, 101, and 102); and

  adapting said filter used to filter said successive phase difference values based on average control values (Fig.1 element 13, 14, 15, 16, 101, and 102, and column 3 line 43 – column 4 line 23 and column 5 equation 8) determined from said successive control values.

- With regard claim 2, Tanaka further discloses detecting a trend in said average control values and determining a filter state based on said trend in said average control values (column 3 line 58 – column 4 line 18 and column 5 line 40 – column 6 line 25).

- With regard claim 3, Tanaka further discloses selecting a fast filter setting for said filter when said trend indicates that said average control values have not stabilized (column 3 line 58 – column 4 line 18 and column 5 line 40 – column 6 line 25).

- With regard claim 4, Tanaka further discloses a slow filter setting for said filter when said trend indicates that said average control values have stabilized (column 5 line 40 – column 6 line 25).
- With regard claim 5, Tanaka further discloses determining difference values between successive ones of said average control values (Fig.1 elements 13-15, column 4 lines 1-18, and column 6 lines 42-65), and wherein adapting said filter based on said average control values determined from said successive control values comprises adapting said filter based on processing said difference values (Fig.1 elements 101, 102, and column 5 line 56 – column 6 line 25).
- With regard claim 6, Tanaka further discloses wherein adapting said filter based on processing said difference values comprises:

  integrating a number of said difference values to determine an integrated value of said number of said difference values (Fig.1 element 13-15, column 4 lines 1-18, and column 5 lines 55-65); and

  adapting said filter based on said integrated value (Fig.1 elements 16, 101, and 102, and column 5 line 56 – column 6 line 25).

  Note that Tanaka discloses the claimed invention except for "a integrating a number of said difference values". It would have been obvious to one having ordinary skill in the art at the time the invention was made to "use an average filter (Fig.1 element 15 and column 4 lines 1-18) to integrate a number of said difference values" since the examiner takes Official Notice of the equivalence of "a average filter" and "an integrating component" for their use in the electronic

circuitry art and the selection of any of these known equivalents to "integrate or averaging an input signal" would be within the level of ordinary skill in the art.

- With regard claim 7, Tanaka further discloses wherein adapting said filter based on said integrated value comprises setting said filter to a slow filter state if said integrated value is below a defined threshold (Fig.1 element 16, column 4 lines 1-23, and column 5 line 56 – column 6 line 25).
- With regard claim 10, which is a method of controlling a phase-locked loop (PLL) claim related to claim 1, all limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 11, which is a method of controlling a phase-locked loop (PLL) claim related to claims 3 and 4, all limitation is contained in claims 3 and 4. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 13, which is a method of controlling a phase-locked loop (PLL) claim related to claim 6, all limitation is contained in claim 6. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claims 14 and 15, Tanaka further discloses wherein said adapting said filter characteristic of said digital filter based on said integrated value comprises changing from a relatively slow filter time constant to a relatively fast filter time constant if said integrated value is above a first integrated value threshold and changing back to said relatively slow filter time constant if said integrated value falls below a second integrated value threshold (column 5 line 56 – column 6 line 25).

Tanaka's reference discloses that the output signal of the averaging circuit 15 is supplied to the data determining unit 16 so as to determine whether or not the output signal of the averaging circuit 15 is large toward a threshold level. The PLL controller 102 selects the parameters of the loop range, the frequency control width, and the control time interval of the PLL corresponding to the output signal of the data determining unit 16 so as to control the PLL filter 11. It also states that with respect to the control time interval, the time constant of the loop filter 11 is not always constant. Instead, the time constant is varied at predetermined time interval so as to maintain the stability and quick response of the characteristics of the PLL. The time constant can be set up in various manners. For example, when the setup data is selected from the memories 101 and 103 corresponding to the output signal of the data determining device 16, the operation of the PLL can be controlled with flexibility. It has not specifically disclosed the limitation "changing from a relatively slow filter time constant to a relatively fast filter time constant if said integrated value is above a first integrated value threshold". One of ordinary skill in the art would have expected the applicant's limitation " changing from a relatively slow filter time constant to a relatively fast filter time constant if said integrated value is above a first integrated value threshold" to perform equally well if it is implemented into the Tanake's carrier phase synthchronizing circuit (Fig.1 11, 13-16, 101, and 102) since " changing from a relatively slow filter time constant to a relatively fast filter time

constant" or vice verse and "if said integrated value is above a first integrated value threshold" or vice verse are merely a design choice.

- With regard claim 16, the limitation of "a defined duration of time" can further be found in column 6 lines 12-20. All other limitation is contained in claim 15. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 18, all limitation is contained in claim 15. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 24, Tanaka discloses a controllable oscillator (Fig.1 element 9) providing an output signal at a frequency proportionate to an oscillator control signal (Fig.1 element 11 output, g(nT)); and

  a phase detector providing a phase error signal (Fig.1 elements 8 and 10 and Fig.2 elements 4 and 10) by detecting a phase difference between an input signal and said output signal (Fig.1 element 6 output and element 9 output);

  an adjustable loop filter providing control values based on filtering said phase error signal (Fig.1 element 11);

  a control circuit providing the oscillator control signal (Fig.1 elements 9 and 11) responsive to said control values; and

  control logic to control a filter characteristic of said loop filter (Fig.1 elements 101 and 102, column 4 lines 1-18, and column 6 lines 1-25) based on an average control value determined from successive ones of said control values to minimize clock deviations in said output signal (Fig.1 elements 13-16, column 3 line 58 – column 4 line 18 and column 5 line 40 – column 6 line 25).

- In regard claim 25, Tanaka further discloses wherein said control logic is operable in one of a defined number of states (column 4 lines 3-18), and further wherein said control logic adjusts said filter characteristic of said loop filter based on a current state of said control logic (column 5 line 56 – column 6 line 25). It is inherent that the control logic is operable in at least one of the two states, lock state and unlock state (stable or unstable states). Tanaka's reference in column 5 line 56 – column 6 line 25 clearly describes how the filter 15 characteristics being adjust by the PLL controller 102 (control logic) based on its current state.
- In regard claim 26, Tanaka further discloses wherein said control logic transitions from a first state to a second state based on at least one characteristic of said average control values (column 6 lines 2-25).
- In regard claim 32, Tanaka further discloses wherein said loop filter comprises a digital loop filter adapted to output said control value in a digital format (Fig.1 element 11).

  Tanaka's reference describes that the A/D converter 2 converts the quasi-coherent orthogonal input signal as an analog signal into a digital signal (column 3 lines 46-48), thereafter, all processing steps are in digital form. It is inherent that the loop filter 11 is a digital loop filter (with digital output signal g(nT), formula 6 and 7).
- With regard claim 37, all limitation is contained in claim 26. The explanation of all the limitation is already addressed in the above paragraph.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 34, 35, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (US 5,909,148) in view of Wilhelmsson et al. (US 6,353,647).

- With regard claims 34 and 35, Tanaka discloses the claimed invention except for specifically teaching a DAC with input from a digital value generated from said loop filter and a VCO controlled by the DAC generated control viltage instead of a NCO 9 receiving a digital input value g(nT) from said loop filter 11. Wilhelmssons' reference shows that a DAC (Fig.12 element 3) with input from a digital value generated from said loop filter (Fig.12 element 44) and a VCO controlled by the DAC generated control viltage (Fig.12 element 9) is an equivalent structure known in the art. Therefore, because these two "the NCO" and "the DAC with VCO" were art-recognized equivalents at the time the Invention was made, one of ordinary skill in the art would have found it obvious to substitute (DAC and VCO) for (NCO).
- With regard claim 39, Tanaka discloses all of the limitation as described in the above paragraph except for specifically teaching the limitation wherein said control logic comprises a digital processor.

However, Wilhelmsson et al. teach wherein said control logic comprises a digital processor (Fig. 10, 12, and 14, and column 9 lines 59-66) in order to reduce the board size so that the circuit cost is reduced.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Tanaka's control circuits (Fig.1 elements 11, 14-16, 101, and 102) in view of Wilhelmssons' filter control circuit (Fig.12 elements 13 and 44) in order to reduce the board size so that the circuit cost is reduced.

7. Claims 12 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (US 5,909,148) in view of Glass (US 5,619,543).

- In regard claim 12, Tanaka discloses all of the limitation as described in the above paragraph except for specifically teaching that digital filter is a proportional-integral (P-I) digital filter.

  Glass discloses a digital phase-locked loop filter with a proportional-integral type digital PLL filter (Fig.3 and 4, and column 2 line 60 – column 4 line 23) in order to use a relatively high coefficient K_L to ensure fast control during the initial phase, and once the communication is established to decrease coefficient K_L (and more generally the filtering coefficients K) to carry out small corrections and to ignore high instantaneous variations normally corresponding to non-repetitive parasitic pulses so that the jitter is reduced and signal quality is improved.

  It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Tanaka's filter circuit in view of Glass's proportional-integral type digital PLL filter in order to eliminate the jitter and improve the signal quality.

- In regard claim 33, which is a PLL claim related to claim 12, all limitation is contained in claim 12. The explanation of all the limitation is already addressed in the above paragraph.

Allowable Subject Matter

8. Claims 8, 9, 17, 19-23, 27-31, 36, 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

10. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2634

Ted M. Wang

KEVIN BURD
PRIMARY EXAMINER